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# A Signal Anti-reduction System for Power Line Communication

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**ABSTRACT**

A new communication system is suggested using a single-phase full-bridge inverter with high efficiency ferrite core for power line communication (PLC). The conventional system has a decreasing signal voltage problem due to internal resistance. The proposed system has almost zero internal impedance and replaces a linear amplifier.

**Keywords :** Power Line Communication, Inverter Application

## 1. Introduction

According to the developing information society, the implementation of power line communication was a great decision by the electronics industry, especially for building automation, home automation and LAN systems. Though many attempts were made, none were successful until the late 1970's [1]. Home automation will cut energy costs by allowing precise, intelligent control over energy usage[2][3]. A PLC system using a spread spectrum technique is designed to overcome disturbances especially narrow-band impairments[4][5]. Computers, power supplies, inverters, converters and motor drive systems are all examples of loads that have a capacitor component at home or in the business world. These capacitors increase the leakage carrier current due to their low impedance against the carrier frequency in the PLC system. In the conventional system, due to internal resistance, this leakage current causes the signal voltage to be decreased by about 20Ω during transmission[6]. To overcome this problem, blocking filters with high Q factor can be connected to block the effect of the load capacitance on the carrier frequency. However, this method requires blocking filters for each piece of equipment. This paper proposes a special switching amplifier with high efficiency ferrite core as signal anti-reduction equipment.

## 2. Simple mathematical modeling

Since proposed switching amp that has small internal resistance reduces that problem of the signal reduction. In order to solve these problems, the amplifier of a transceiver must have a low internal resistance and be able to supply reactive power. A block diagram of the proposed system is given in Fig. 1. A switching amplifier composed of a single-phase full-bridge inverter is inserted between the transmitter and the receiver. As shown in this figure, the switching amplifier replaces a linear amplifier. Furthermore, we suggest using one with a high efficiency

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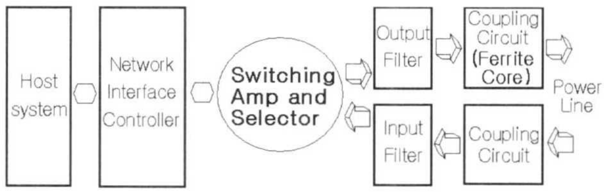


Fig. 1 Block diagram of a PLC system

ferrite core. This core phenomenonally reduces the leakage reactance of the coupling circuit. This means that there is no reduction in the signal due to internal resistance or leakage inductance. This is depicted in Fig 2, where $r$ is the internal impedance of the amp, $R$ is the line resistance, $L$ is the inductance, $C$ is the line capacitance, $C_2$ is the load capacitance, $v_s$ is the signal voltage and $v_p$ is the power voltage.

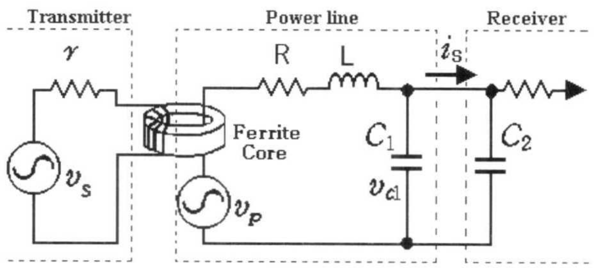


Fig. 2 A load equivalent circuit

In Fig.2 the noise effect, impedance characteristic and signal reduction must be considered in the power line. Using a Laplace Transform to obtain the load voltage between the two terminals; the load current $I_S$ is given by:

$$I_S(s) = sC_2V_s(s)/[LC_es^2 + (r+R)C_es + 1] \quad (1)$$

where $C_e = C_1 + C_2$ . Therefore the signal current is obtained under the influence of the capacitor $C_2$ in receiving node.

## 3. Simulation and Experimental Result

To verify the prediction, a switching amplifier system with low internal resistance is proposed. It can provide reactive power and has low impedance between the transmitting and the receiving node. The new system consists of a MOS Field Effect Transistor(MOSFET). Unlike a linear amplifier, the full-bridge switching amplifier has low internal resistance and is able to provide reactive power. A bridge inverter can replace the linear amplifier found in a conventional amplifier system. In the conventional system, the internal resistance of the amplifier is between 20~50Ω. However, it is almost zero for the MOSFET in operating a saturation region in the proposed method. Furthermore, this system has high efficiency core for transforming a signal to a power line. This high performance ferrite core reduces the leakage inductance and the weakening of the signal. Therefore the line impedance decreases. Fig. 3 shows the block diagram of a new amplifier for spread spectrum communication (SSC) using phase information [1][2][4].

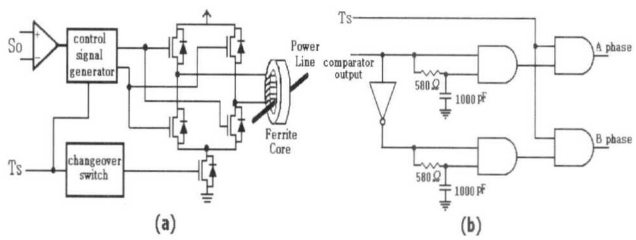


Fig. 3 Block diagram of the new amplifier for SSC and control signal generator

This system adopts a FET which switches much faster than a normal transistor. "So" is a signal from a chip set for SSC. This signal is converted into the control signal by a comparator. Part of the control signal generator is shown in Fig. 3(b). The comparator signal changes the inverter-switching signal. At this time "Ts" signal synchronizes the overall system. Adding a switching device on the load line prevents low impedance between the transmitting and receiving node as shown in Fig. 3(a). Therefore, if the switch is on, the switching amplifier system running full-bridge inverter can transmit the data. When the switch is off, the new system is waiting to receive a signal. The ferrite core coupling also reduces the leakage flux signal between transmitter and receiver.

## 4. Simulation and Experimental Results

The simulation and experiment were done using a PLC system. The simulation results in Fig. 4 show the waveform from the conventional system with load capacitor and internal resistance. This simulation uses very simple circuits so that the real system equivalents will not be too complex.

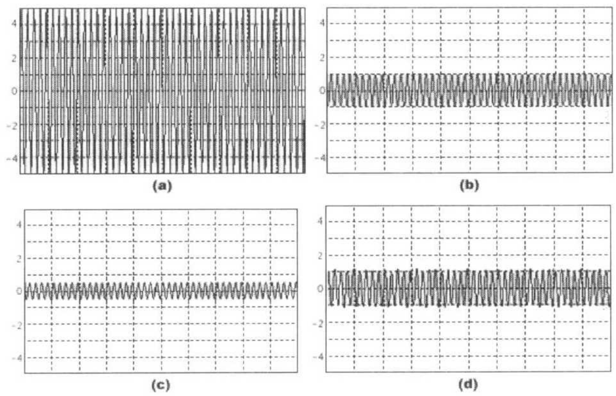


Fig. 4 Input waveform of the transmitting and receiving node
(a) Transmitted signal (C=0.0087 $\mu$ F R=0.62 $\Omega$ r=25 $\Omega$ )
(b) Received signal (C=0.0087 $\mu$ F R=0.62 $\Omega$ r=25 $\Omega$ )
(c) Received signal (C=0.0158 $\mu$ F R=0.62 $\Omega$ r=25 $\Omega$ )
(d) Received signal (C=0.0158 $\mu$ F R=0.62 $\Omega$ r=0.02 $\Omega$ )

Fig. 4(b) shows the voltage of the receiving node at 1V in case of low capacitor load. Capacitors in the system reduce the transmission signal as shown in Fig. 4(c). Because it is the load capacitor, Fig. 4(c) shows that the received voltage of the amplifier system having the internal resistance of r=25 $\Omega$ is low at less than 1Vp-p. If the value of internal resistance is small, the voltage will be more than 2Vp-p – a 100% improvement. Therefore, as shown in Fig. 4(d), the voltage drop is decreased when the internal resistance is reduced as much as possible. Experimental waveforms are showed in Fig. 5~7. This experiment adopts the Intellon SSC P400 Network IC [6]. The SSC P111 PL Media Interface IC provides the output signal amplification. The coupling of the transmission signal is obtained by SN-20 made by Samhwa Co. [5][6]. In this experiment, we used the power line of the building, which powers many computers, inverters, and converter systems. As explained before, a ferrite core coupling is used in this experiment. In this experiment the load consists of many computers and converters. The voltage of the receiving node is measured f1 in each case. Fig. 5 shows the transmitting and receiving waveforms of the conventional and the proposed system.

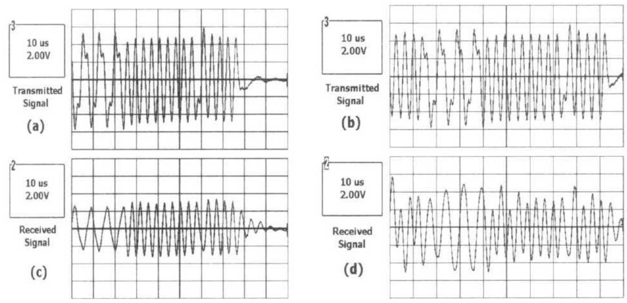


Fig. 5 Comparison of the signal on the power lone with no load
(a) (c) The conventional system
(b) (d) The proposed system

The receiving voltage waveform in Fig. 5(b) is bigger than in Fig. 5(a). So the proposed system has a low influence on the load of the pre-existing power line. The received signal is not exactly the same as the source signal because of the power line filter, stray inductance and the capacitor. Fig. 6 shows a comparison of the received signals where the power rate compensation capacitor of 50 $\mu$ F is connected to the midpoint between the transmitting and receiving nodes. As shown in Fig.6 (a) we can obtain 2$V_{P\text{-}P}$ as a received signal voltage, however we cannot get exact information because of the inexact zero crossing signal.

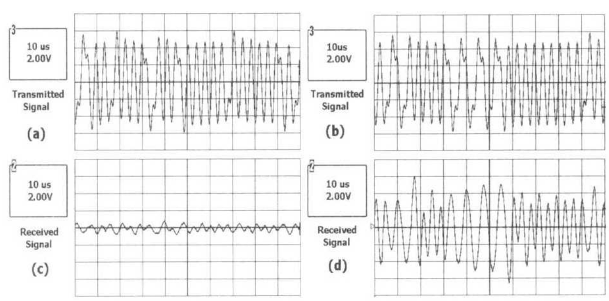


Fig. 6 Comparison of the signal on the power line with load
(a) (c) The conventional system
(b) (d) The proposed system

On the other hand, the voltage of the proposed system shows 8Vp-p. Thus, performance has been improved by 400%. Since a signal reduction cannot be completely avoided at high frequency, the received voltage could not be greater than 10Vp-p. However, the proposed system also received effective data excellently. A Fourier transformed signal is shown in Fig 7(a) and 7(b) obtained from Fig 7(c) and 7(d), respectively. This shows that the magnitude of the meaningful signal has increased.

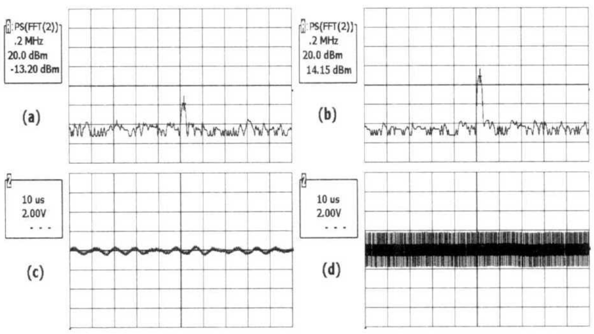


Fig. 7 A load with blocking filter
(a) (c) The conventional system
(b) (d) The proposed system

The y-axis represents frequency and the x-axis represents time. As shown Fig 7(a), there is no switching noise. However, the transmitted signal is smaller than Fig. 7(b). The magnitude of the signal is -13.20 dB. For the proposed system, even though there is a lot of switching noise across the whole frequency, the magnitude of the transmitted data is 14.15 dB. We can say that the signal is transmitted well to the receiver. The transfer speed can be increased if we use a high speed switching device greater than 1 MHz.

## 5. Conclusions

This paper shows the PLC system can be analyzed as a simple R-L-C circuit. Using a single-phase full-bridge inverter as a switched amplifier can reduce the signal reduction caused by an inductor or capacitor. The simulations and experiments in this paper clearly demonstrate the effectiveness of the proposed inverter. If we use a faster switch, the system response will increase.

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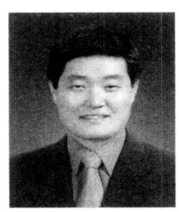

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